Ordering number : EN*5127A

CMOS LSI

LC78836M

Digital Audio 16-bit D/A Converter with On-Chip Digital Filters

Preliminary

Overview

The LC78836M is a 16-bit CMOS D/A converter that includes 8× oversampling filters on chip. It is pin compatible with the LC78835M and LC78835KM.

Functions and Features

Digital Filter Block
- 8× oversampling filters: Three FIR filter stages (33rd-order, 13th-order, and ninth-order filters)
- De-emphasis filter: Support for 32 kHz, 44.1 kHz, and 48 kHz Fs frequencies
- Soft muting
- Noise shaper
- Supports double-speed operation

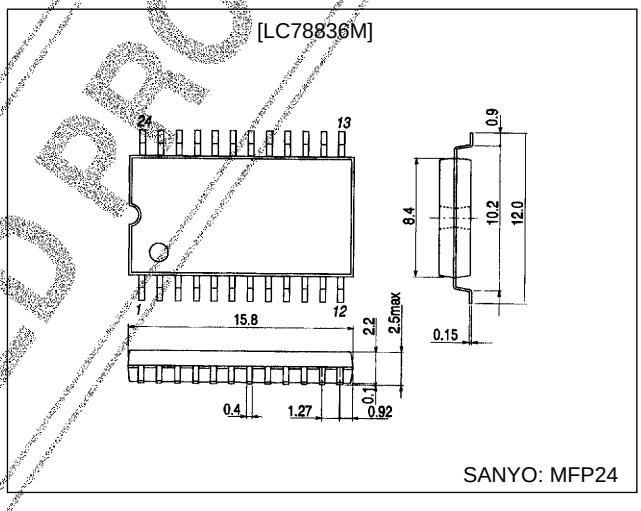
D/A Converter Block
- 16-bit dynamic level shifting D/A conversion
- Two D/A converter channels on a single chip (synchronous outputs)
- On-chip output operational amplifiers
- System clock: Supports 384 fs, 392 fs, 448 fs, and 512 fs clocks

- Single 5 V power supply
- Low-voltage operation (3 V) also possible
- Si-gate CMOS process for low power dissipation

Package Dimension

unit: mm

3155-MFP24



SANYO: MFP24

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input voltage	V_{IN}		–0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		–0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		3.0	5.0	5.5	V
Reference voltage (high)	VrefH		V_{DD} – 0.3		V_{DD}	V
Reference voltage (low)	VrefL		0		0.3	V
Operating temperature	Topr		–30		+75	°C

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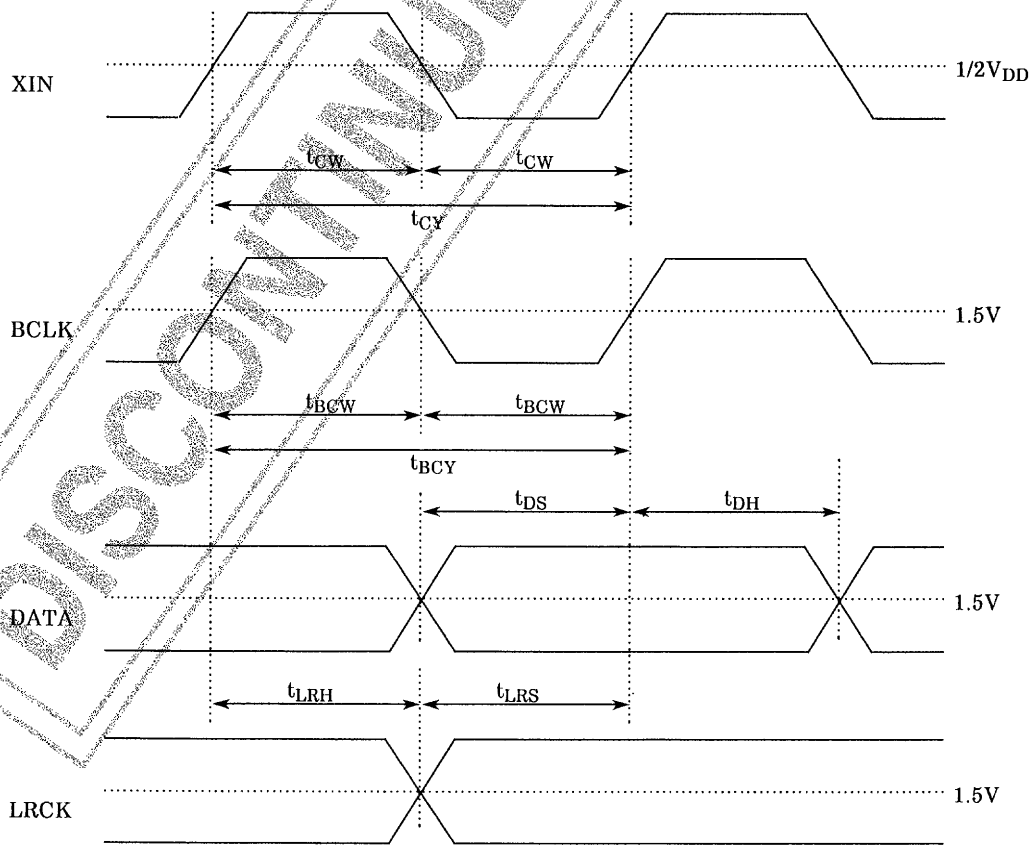
DC Characteristics at Ta = –30 to +75°C, V_{DD} = 3.0 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage (1)	$V_{IH}1$	Pins 3, 4, 5, 6, 7, 13, 14, 15, 16, 17, and 18	2.2			V
Input low level voltage (1)	$V_{IL}1$	Pins 3, 4, 5, 6, 7, 13, 14, 15, 16, 17, and 18			0.8	V
Input high level voltage (2)	$V_{IH}2$	Pin 11	0.7 V_{DD}			V
Input low level voltage (2)	$V_{IL}2$	Pin 11			0.3 V_{DD}	V
Output high level voltage	V_{OH}	Pin 9: I_{OH} = –3 mA	2.4			V
Output low level voltage	V_{OL}	Pin 9: I_{OL} = 3 mA			0.4	V
Input leakage current	I_L	Pins 3, 4, 5, 6, 7, 11, 13, 14, 15, 16, 17, and 18: V_I = V_{SS}, V_{DD}	–25		+25	µA

AC Characteristics at Ta = –30 to +75°C, V_{DD} = 3.0 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Oscillator frequency	f_X	The XIN pin when a crystal oscillator is used	1.0		25	MHz
Clock pulse width	t_{CW}	When an external clock is input to the XIN pin	18			ns
Clock pulse period	t_{CY}	When an external clock is input to the XIN pin	40		1000	ns
BCLK pulse width	t_{BCW}		60			ns
BCLK pulse period	t_{BCY}		120			ns
Data setup time	t_{DS}		40			ns
Data hold time	t_{DH}		40			ns
LRCK setup time	t_{LRS}		40			ns
LRCK hold time	t_{LRH}		40			ns

Audio Input Waveforms



Electrical Characteristics (1)

at Ta = 25°C, AV_{DD} = DV_{DD} = VrefH = 5.0 V, AGND = DGND = VrefL = 0 V unless otherwise specified

Parameter	Symbol	Conditions	min	typ	max	Unit
DAC resolution	RES			16		bits
Total harmonic distortion	THD	For f = 1 kHz, 0 dB*1			0.08	%
Dynamic range	DR	For f = 1 kHz, –60 dB	92	94		dB
Crosstalk	CT	For f = 1 kHz, 0 dB			–85	dB
Signal-to-noise ratio	S/N	JIS-A	96	100		dB
Full-scale output voltage	VFS		2.8	3.0	3.2	Vp-p
Power dissipation	Pd	*2		90	135	mW
Output load resistance	RL	Pins 21 and 23	5			kΩ

Note: 1. 0 dB means full scale.
2. XIN amplitude (pin 11): 1.5 to 3.5 V, f_X = 16.9344 MHz
The test circuit should be based on the sample application circuit.

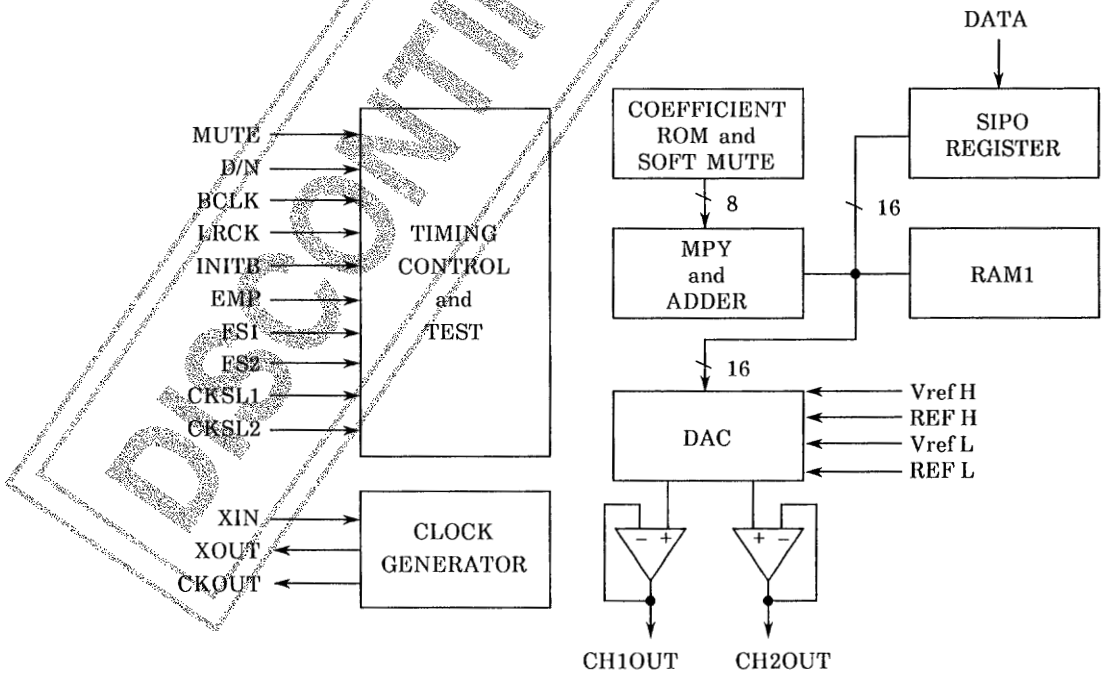
Electrical Characteristics (2)

at Ta = 25°C, AV_{DD} = DV_{DD} = VrefH = 3.0 V, AGND = DGND = VrefL = 0 V unless otherwise specified

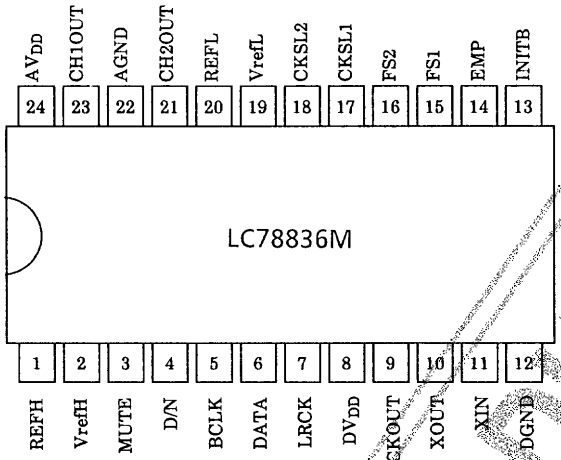
Parameter	Symbol	Conditions	min	typ	max	Unit
DAC resolution	RES			16		bits
Total harmonic distortion	THD	For f = 1 kHz, 0 dB*1			0.10	%
Dynamic range	DR	For f = 1 kHz, –60 dB	90	92		dB
Crosstalk	CT	For f = 1 kHz, 0 dB			–85	dB
Signal-to-noise ratio	S/N	JIS-A	94	98		dB
Full-scale output voltage	VFS		1.65	1.8	1.95	Vp-p
Power dissipation	Pd	*2		20	30	mW
Output load resistance	RL	Pins 21 and 23	30			kΩ

Note: 1. 0 dB means full scale.
2. XIN amplitude (pin 11): 0.9 to 2.1 V, f_X = 16.9344 MHz
The test circuit should be based on the sample application circuit.

Block Diagram



Pin Assignment

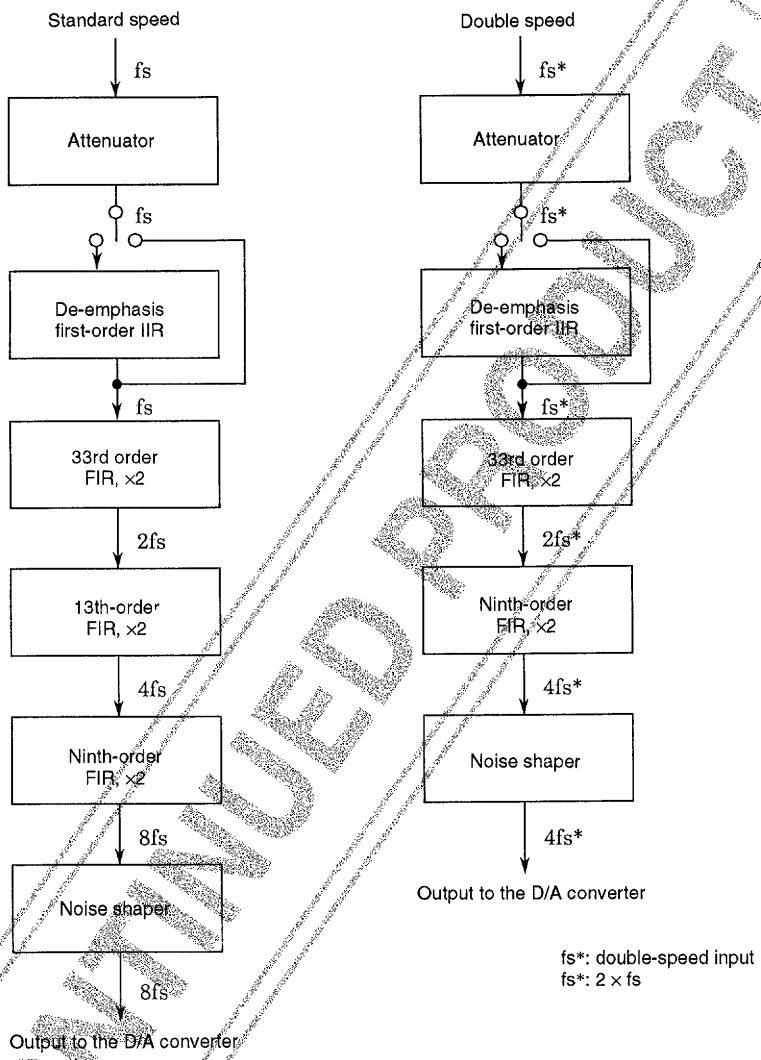


Pin Functions

Pin No.	Symbol	Function
1	REFH	High-level reference voltage Normally connected through a capacitor to AGND.
2	VrefH	High-level reference voltage input
3	MUTE	Muting signal input The soft muting function is turned on by a high input.
4	D/N	Standard/double-speed mode switching input Double-speed operation when high, standard when low.
5	BCLK	Bit clock input
6	DATA	Digital audio data input Input is in a twos-complement MSB-first format.
7	LRCK	LR clock input CH1 is input when this pin is high, CH2 when low.
8	DV_{DD}	Digital system power supply
9	CKOUT	Clock output In 392 fs mode: outputs a 196 fs clock In other modes: outputs a clock with the XIN frequency
10	XOUT	Crystal oscillator output (system clock output)
11	XIN	Crystal oscillator input (system clock input)
12	DGND	Digital system ground
13	INITB	Initialization signal input The LSI is initialized when this pin is set low.
14	EMP	De-emphasis filter on/off switching The filter is turned on when this pin is set high, off when set low.
15	FS1	De-emphasis filter mode (32, 44.1, or 48 kHz) selection FS1: L, H, H, L FS2: L, L, H, H fs: 44.1 kHz, 32 kHz, 48 kHz
16	FS2	
17	CKSL1	System clock selection CKSL1 / CKSL2 / System clock L / L / 384 fs L / H / 392 fs H / L / 448 fs H / H / 512 fs
18	CKSL2	
19	VrefL	Low-level reference voltage input
20	REFL	Low-level reference voltage Normally connected through a capacitor to AGND.
21	CH2OUT	CH2 analog output
22	AGND	Analog system ground
23	CH1OUT	CH1 analog output
24	AV_{DD}	Analog system power supply

Operating Description

1. Digital Filters
   The LC78836M performs the following calculations.

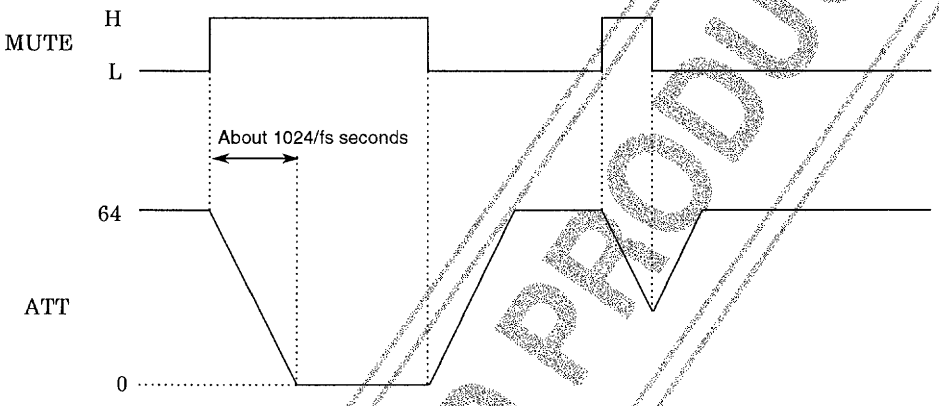


- Oversampling
  The oversampling circuit consists of 2× interpolation filters (implemented as FIR filters) connected in series. In standard-speed operation, the circuit implements 8× oversampling by connecting three stages of FIR filters (33rd,13th, and ninth orders) in series. In double speed operation, the circuit implements 4× oversampling by connecting two stages of FIR filters (33rd and ninth orders) in series. See page 9 for the filter characteristics.
- De-emphasis
  The LC78836M implements digital de-emphasis with a first-order IIR filter. The filter coefficients correspond to sampling frequencies (fs) of 32, 44.1, and 48 kHz. (The frequencies are doubled in double-speed operation.) See page 10 for the filter characteristics when de-emphasis is on.
  — De-emphasis on/off switching
  De-emphasis on: EMP = high
  De-emphasis off: EMP = low
  — Filter coefficient selection

FS1	L	H	H	L
FS2	L	L	H	H
fs	44.1 kHz		32 kHz	48 kHz

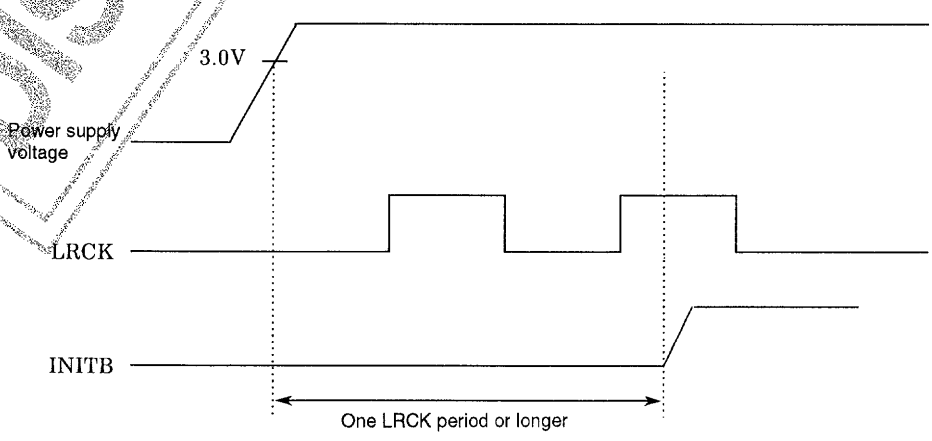
- Soft muting
  Soft muting is implemented using the on-chip digital attenuator.
  The attenuator attenuation is given by the following formula.
  20 Log (ATT/64) dB

  Here, ATT is an integer between 0 and 64 inclusive. However, the attenuation is –∞ when ATT = 0. When the MUTE pin is set high, the ATT value is reduced one level at a time towards zero, and the attenuation changes, moving towards –∞. When the MUTE pin is set low, the ATT value is increased one level at a time towards 64, and the attenuation changes, moving towards 0 dB. The time required for the soft mute function to complete is about 1024/fs.



- Noise shaper
  The LC78836M uses a first-order noise shaper to reduce re-quantization noise in the output of the DF calculations.
- Double-speed support
  The LC78836M supports double-speed CD playback when the D/N pin is set high. In this mode, the BCLK, LRCK, and DATA inputs should be input with twice the frequencies they have in standard-speed mode. Note that the system clock (the XIN pin clock) has the same frequency as it does in standard-speed mode. The LC78836M supports double-speed operation when the system clock is a 384 fs or 512 fs clock, but does not support this mode for 392 fs and 448 fs clocks. Since the LC78836M enters test mode for these settings, they should not be used.
  Standard-speed mode: D/N pin = low
  Double-speed mode: D/N pin = high

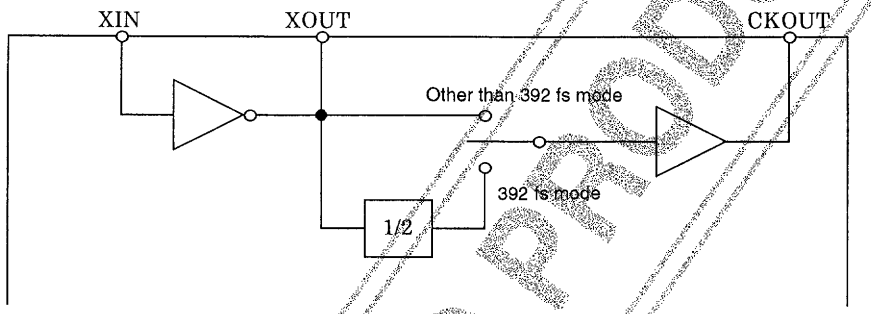
2. Initialization
   The LC78836M must be initialized when power is first applied or when the system clock is switched. Initialization is executed by setting the INITB pin low. While that pin is low, after the power supply voltage stabilizes, input the XIN, BCLK, and LRCK signals, and wait at least one LRCK period, as shown in the figure below.
   When INITB is low, all 16 bits of the digital filter outputs will be zeros, and the D/A converter outputs (CH1OUT and CH2OUT) will be analog 0 (a potential essentially equal to $(V_{REFH} + V_{REFL})/2$).



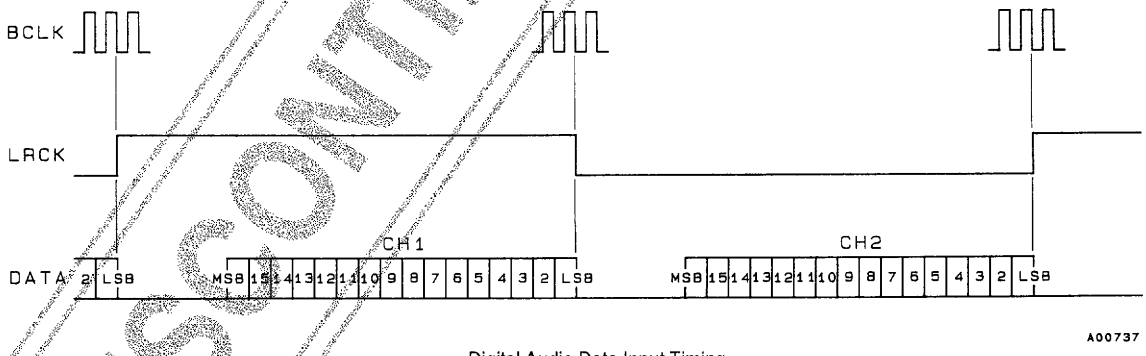
3. System Clock
   The LC78836M supports four system clocks: 384 fs, 392 fs, 448 fs, and 512 fs. The CKSL1 and CKSL2 pins select the clock used.

CKSL1	CKSL2	System clock
L	L	384 fs
L	H	392 fs
H	L	448 fs
H	H	512 fs

   • CKOUT pin
   For a 392 fs clock: Outputs a 196 fs clock (system clock/2)
   All other clocks: Outputs the system clock



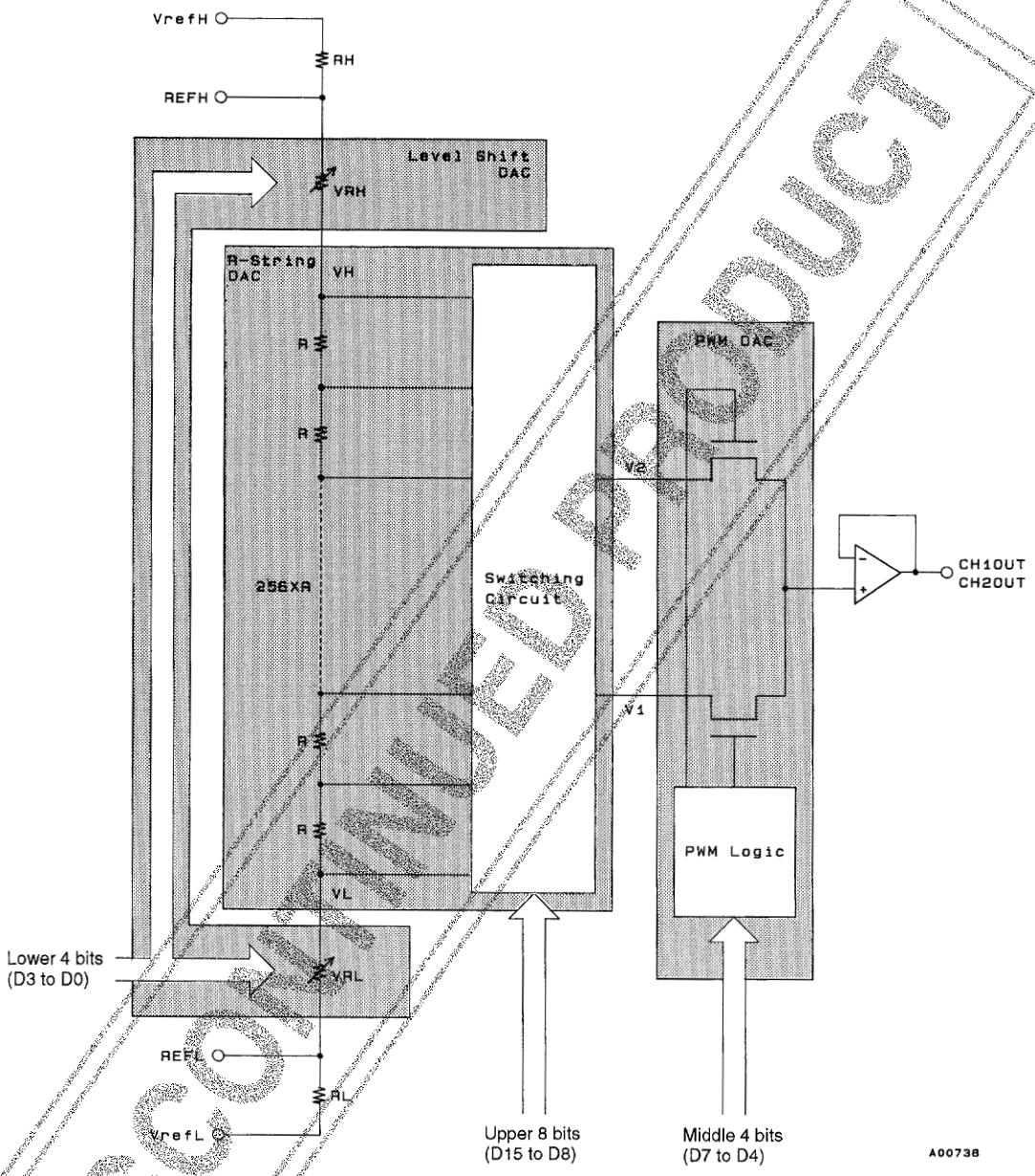
4. Digital Audio Data Input
   The digital audio data is a 16-bit serial signal in an msb-first twos complement format. The 16-bit serial data is input from the DATA pin to an internal register on the rising edge of BCLK, and is latched on the next LRCK rising or falling edge.



Digital Audio Data Input Timing

5. D/A Converter Block

The LC78836M incorporates an independent 16-bit D/A converter and an operational amplifier for signal output for each channel (CH1 and CH2). It adopts a dynamic level shifting conversion technique that uses a resistor-string D/A converter, a PWM (pulse width modulation) D/A converter, and a level shifting D/A converter. (See figure.)



- Resistor-string D/A converter

  This is an 8-bit D/A converter in which a total of 256 (= 2^8) unit-resistance resistors are connected in series and the potential applied to the ends of that resistor string is voltage divided into 256 equal intervals. Of these resistor-divided potentials, two adjacent potentials, V1 and V2, are selected by a switching circuit according to the value of the upper 8 bits of the data. These two potentials are output to the PWM D/A converter. Note that these potentials are related as follows:

  $V2 - V1 = (VH - VL)/256$

- PWM D/A converter

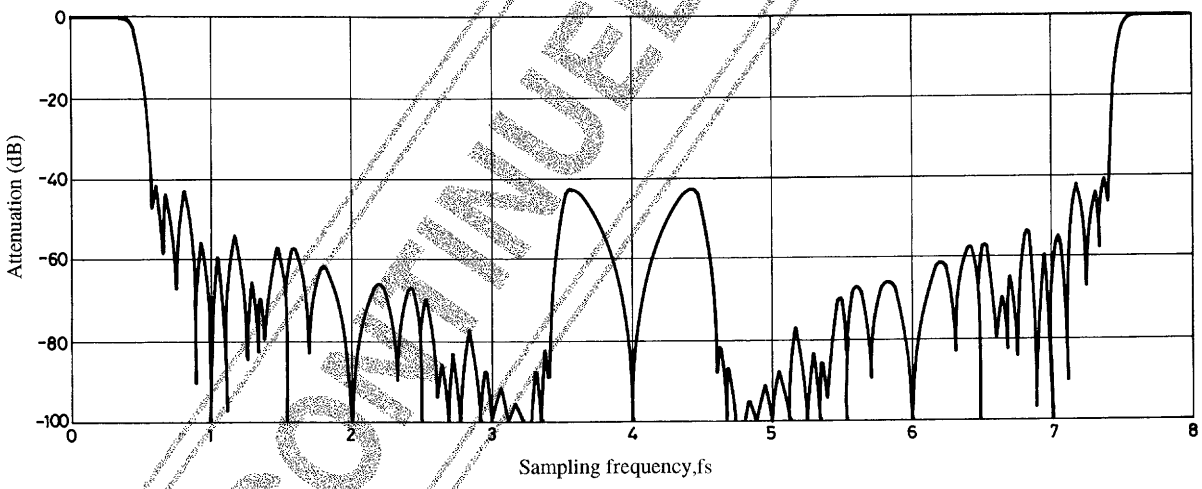
  This is a 4-bit D/A converter that divides (by 16) the interval between the two potentials, V1 and V2, output by the resistor-string D/A converter. This circuit outputs one or the other of the V1 and V2 potentials from the CH1OUT (or CH2OUT) pin according to the value of the middle 4 bits of the data (D7 to D4).

- Level shifting D/A converter
  This 4-bit D/A converter is implemented by connecting the variable resistors VRH and VRL in series at the ends of the resistor-string D/A converter resistors. The values of the VRH and VRL variable resistors are modified according to the value of the low-order 4 bits of the data (D3 to D0) as follows:
  — The value of VRH + VRL is held fixed regardless of the value of the data.
  — The values of VRH and VRL are changed in R/256 unit steps (where R is the value of the resistor-string D/A converter unit resistors) over the range zero to 15·R/256.
  This causes the resistor-string D/A converter V1 and V2 outputs to change in ΔV/256 steps (where ΔV = (VH –VL)/256) over the range 0 to 63 × ΔV/256 according to the value of the lower 4 bits of the data.
- VrefH/L and REFH/L pins
  The VrefH/L pins, which provide a reference voltage to the resistor string, are normally set to VrefH = AV_{DD} and VrefL = AGND. Note that capacitors (about 10 µF) should be connected between REFH and AGND and between REFL and AGND.
  When VrefH is 5.0 V and VrefL is 0 V, the LC78836M outputs its maximum output amplitude as the range 0.5 V (minimum) to 3.5 V (maximum) (3.0 Vp-p) for 0 dB playback according to the built-in RH and RL resistors.

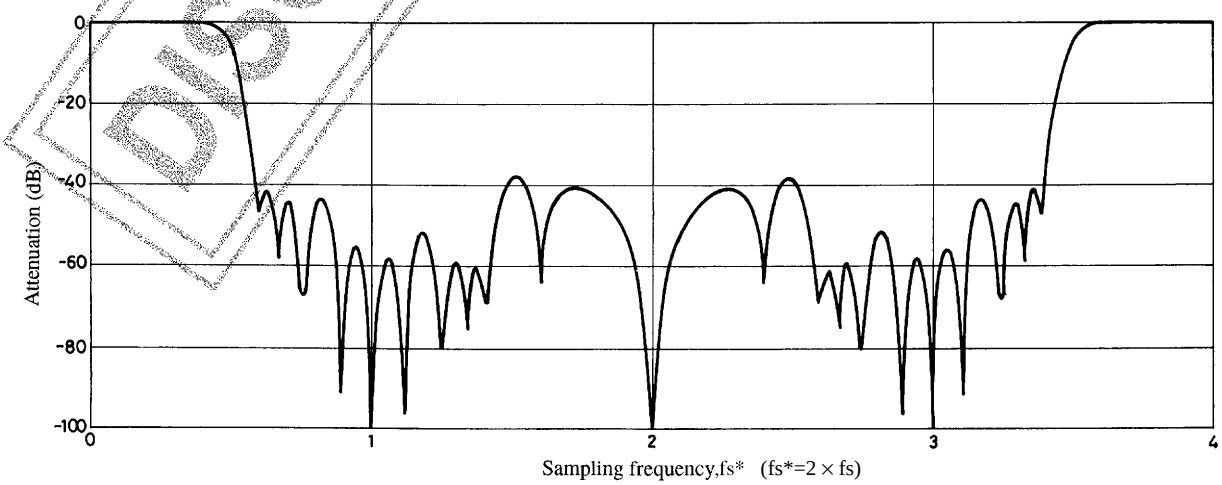
Filter Characteristics (logical values)

Standard speed: 8× oversampling
Double speed: 4× oversampling
Ripple: Less than ±0.1 dB
Attenuation: –40 dB or lower

Standard speed (de-emphasis off)

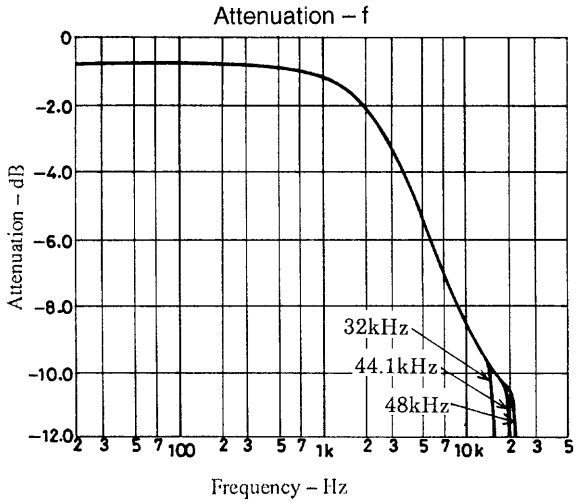


Double speed (de-emphasis off)

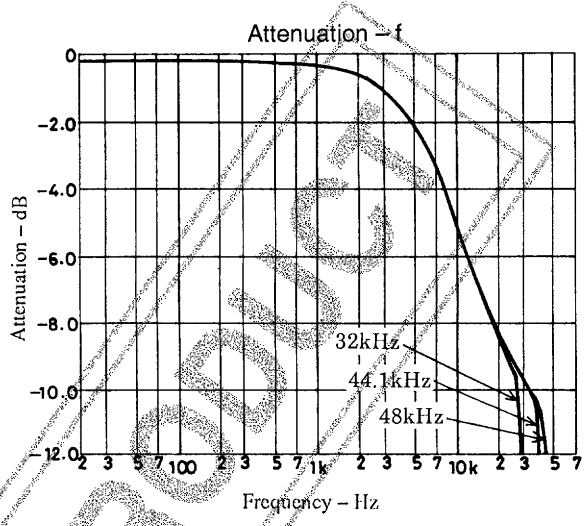


De-Emphasis ON Transient Bandwidth Characteristics

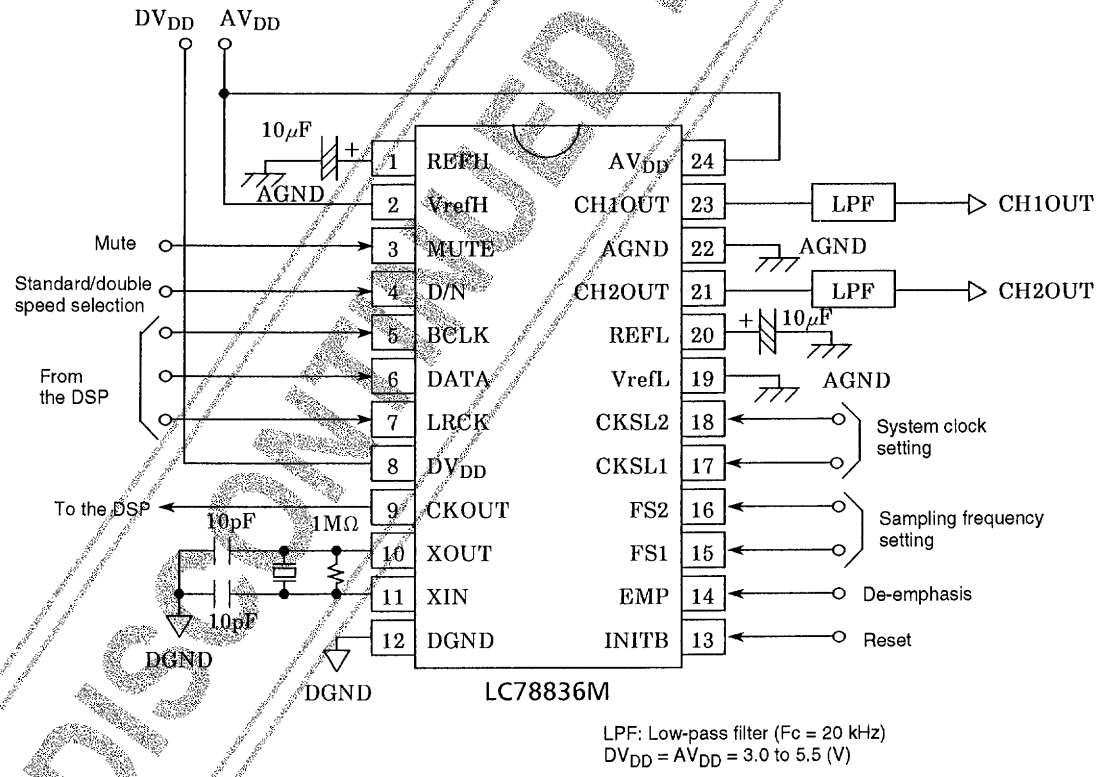
- Standard Speed



- Double Speed



Sample Application Circuit



Note: 1. In the diagram, DV_{DD} and DGND are for the digital system, and AV_{DD} and AGND are for the analog system. DGND and AGND must be connected to the digital system and analog system grounds, respectively.
2. A low-impedance high-stability power supply (equivalent to a commercial three-terminal regulator) must be used for AV_{DD} and VrefH.
3. Since latchup can occur if there is a discrepancy in the pin 8 (DV_{DD}) and pin 24 (AV_{DD}) power supply voltage application timing, application circuits should be designed so that the pin 8 and pin 24 power supply voltages are applied at the same time.
4. Provide the XIN pin clock input quickly after power is applied. The IC may be destroyed if the XIN pin is held fixed at either the high or low level when power is applied.

Power Supply Application Timing

1. The analog power supply (AV_{DD}) and the digital power supply (DV_{DD}) must be turned on at the same time and must be turned off at the same time.

2. If discrepancies in the analog and digital power supply timings cannot be avoided, the timings must fulfill the following conditions.
   - The difference between times when the power supplies rise must be 3 ms or shorter. (See Figure 1)
   - If the time difference is greater than 3 ms, then the power supply that rises (falls) first must have a rise time (fall time) of 5 ms or longer, and the time difference must be less than 50 ms. (See Figure 2)

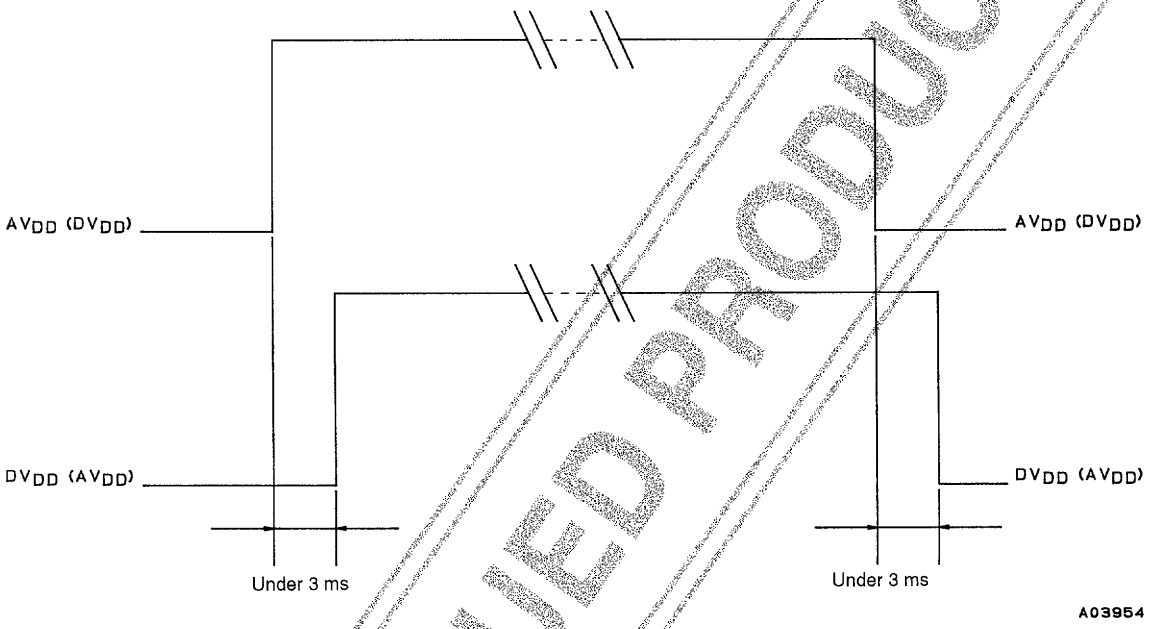


Figure 1

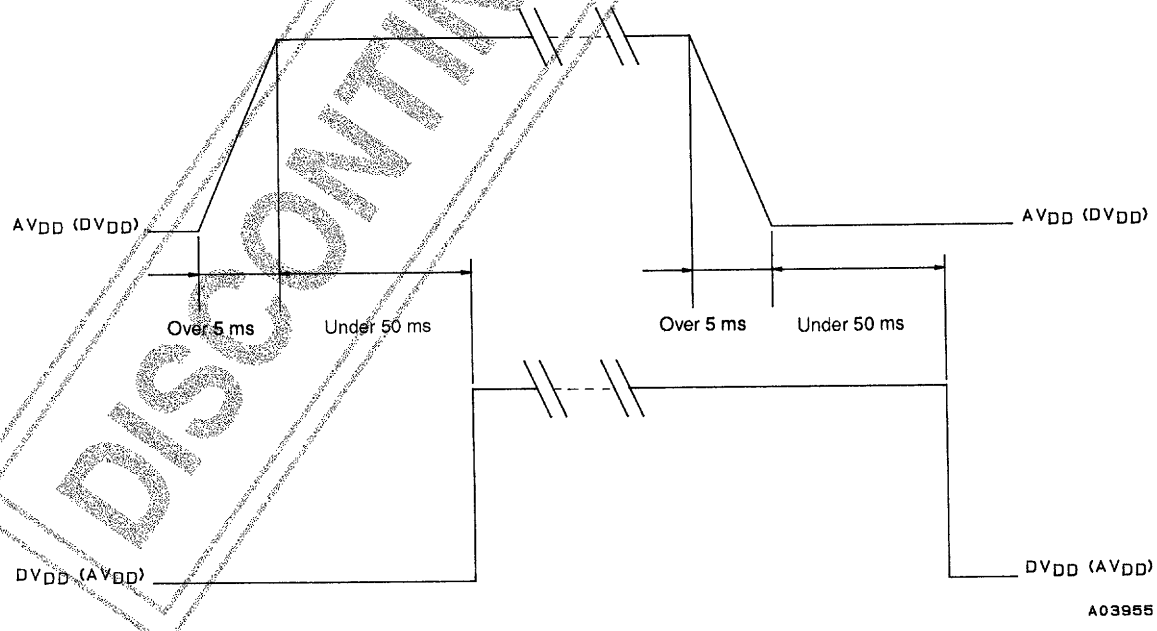


Figure 2

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