LC78836M



# Digital Audio 16-bit D/A Converter

with On-Chip Digital Filters

### Preliminary

### Overview

The LC78836M is a 16-bit CMOS D/A converter that includes  $8\times$  oversampling filters on chip. It is pin compatible with the LC78835M and LC78835KM.

### **Functions and Features**

#### Digital Filter Block

- 8× oversampling filters: Three FIR filter stages (33rdorder, 13th-order, and ninth-order filters)
- De-emphasis filter: Support for 32 kHz, 44.1 kHz, and 48 kHz Fs frequencies
- Soft muting
- Noise shaper
- Supports double-speed operation
- D/A Converter Block
- 16-bit dynamic level shifting D/A conversion
- Two D/A converter channels on a single chip (synchronous outputs)
- On-chip output operational amplifiers
- System clock: Supports 384 fs, 392 fs, 448 fs, and 512 fs clocks

### **Specifications**

#### Absolute Maximum Ratings at Ta = $25^{\circ}$ C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	W <sub>DD</sub> max	and the second	-0.3 to +7.0	V
Input voltage	VIN	المحمور تتوجر	–0.3 to V <sub>DD</sub> + 0.3	V
Output voltage	Vouт		–0.3 to V <sub>DD</sub> + 0.3	V
Operating temperature	Topr		-30 to +75	°C
Storage temperature	🕴 Tstg 🖉 🖉		-40 to +125	°C

#### Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V <sub>DD</sub>	July Contract of C	3.0	5.0	5.5	V
Reference voltage (higb)	VrefH		V <sub>DD</sub> – 0.3		V <sub>DD</sub>	V
Reference voltage (low)	VrefL		0		0.3	V
Operating temperature	Tøpr		-30		+75	°C

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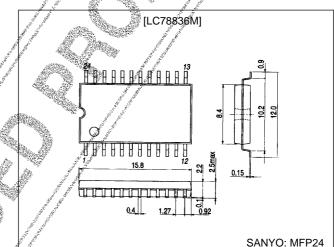
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- Single 5 V power supply
- Low-voltage operation (3 V) also possible
- Si-gate CMOS process for low power dissipation

## Package Dimension

unit: mm 3155-MFP24

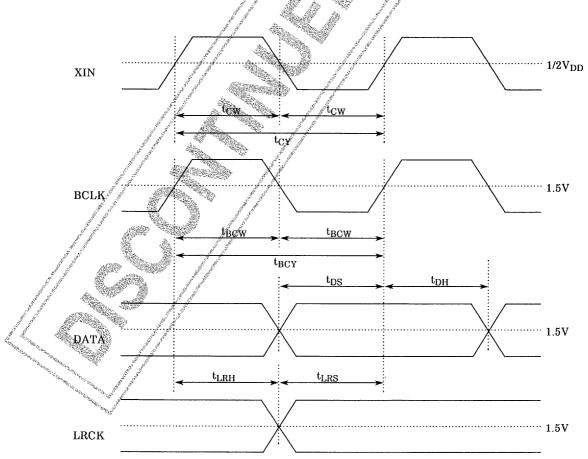


Symbol	Conditions	min	typ	max	Unit
V <sub>IH</sub> 1	Pins 3, 4, 5, 6, 7, 13, 14, 15, 16, 17, and 18	2.2	Če		V
V <sub>IL</sub> 1	Pins 3, 4, 5, 6, 7, 13, 14, 15, 16, 17, and 18			0.8	V
V <sub>IH</sub> 2	Pin 11	0.7 V <sub>DD</sub>		1. No.	V
V <sub>IL</sub> 2	Pin 11	all a set		0.3 V <sub>DD</sub>	V
V <sub>OH</sub>	Pin 9: I <sub>OH</sub> = -3 mA	2,4	all a	and an and a second second	V
V <sub>OL</sub>	Pin 9: I <sub>OL</sub> = 3 mA		C. Star	0.4	) v
IL.	Pins 3, 4, 5, 6, 7, 11, 13, 14, 15, 16, 17, and 18: $V_I = V_{SS}, V_{DD}$	-25		+25	μA
	V <sub>IH</sub> 1 V <sub>IL</sub> 1 V <sub>IH</sub> 2 V <sub>IL</sub> 2 V <sub>OH</sub>	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$V_{IH}1$ Pins 3, 4, 5, 6, 7, 13, 14, 15, 16, 17, and 18     2.2 $V_{IL}1$ Pins 3, 4, 5, 6, 7, 13, 14, 15, 16, 17, and 18     2.2 $V_{IL}2$ Pin 11     0.7 V_{DD} $V_{IL}2$ Pin 11     2.4 $V_{OL}$ Pin 9: I <sub>OL</sub> = -3 mA     2.4 $V_{OL}$ Pin 9: I <sub>OL</sub> = 3 mA     2.4	$\begin{array}{c c c c c c c c c c c c c c c c c c c $

### DC Characteristics at Ta = –30 to +75°C, $V_{DD}$ = 3.0 to 5.5 V, $V_{SS}$ = 0 V

		// ~~~~//	
AC Characteristics	at Ta = -30 to	$v + 75^{\circ}C, V_{DD} = 3.0 \text{ to } 5.5 \text{ V}, V_{SS} = 0 \text{ V}$	
Parameter	Symbol	Conditions typ max	Unit
Oscillator frequency	f <sub>X</sub>	The XIN pin when a crystal oscillator is used 1.0 25	MHz
Clock pulse width	t <sub>CW</sub>	When an external clock is input to the XIN pin	ns
Clock pulse period	t <sub>CY</sub>	When an external clock is input to the XIN pin 40 1000	ns
BCLK pulse width	t <sub>BCW</sub>	60 /	ns
BCLK pulse period	t <sub>BCY</sub>	120	ns
Data setup time	t <sub>DS</sub>	40	ns
Data hold time	t <sub>DH</sub>	40	ns
LRCK setup time	t <sub>LRS</sub>	40	ns
LRCK hold time	t <sub>LRH</sub>	40	ns

#### **Audio Input Waveforms**



#### Electrical Characteristics (1) at Ta = $25^{\circ}$ C, AV<sub>DD</sub> = DV<sub>DD</sub> = VrefH = 5.0 V, AGND = DGND = VrefL = 0 V unless otherwise specified

Parameter	Symbol	Conditions	Conditions		typ	max	Unit
DAC resolution	RES				16		bits
Total harmonic distortion	THD	For f = 1 kHz, 0 dB*1		a start		0.08	%
Dynamic range	DR	For f = 1 kHz, -60 dB		92	94	A Contraction of the second	dB
Crosstalk	СТ	For f = 1 kHz, 0 dB		and the second	Å.	-85	dB
Signal-to-noise ratio	S/N	JIS-A		96	100	$\sim$	dB
Full-scale output voltage	VFS			2.8	3.0	3.2	Ур-р
Power dissipation	Pd	*2	Street Barrier	1	90	185	mW
Output load resistance	RL	Pins 21 and 23	and the second second	6	Sing St		kΩ

Note: 1. 0 dB means full scale.

2. XIN amplitude (pin 11): 1.5 to 3.5 V,  $f_X$  = 16.9344 MHz The test circuit should be based on the sample application circuit.

#### **Electrical Characteristics (2)**

#### at Ta = 25°C, $AV_{DD} = DV_{DD} = VrefH = 3.0 V$ , AGND = DGND = VrefL = 0 V unless otherwise specified

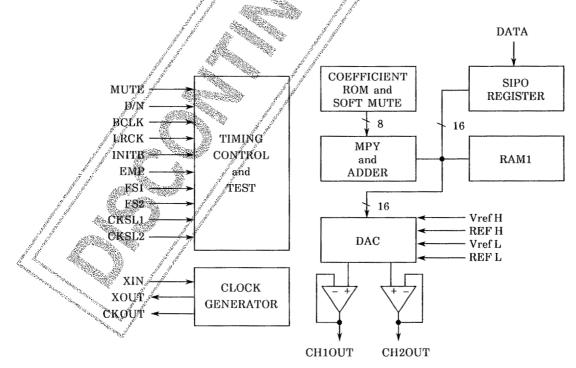
r		// <u>%</u>	<u>i</u> te	)		
Parameter	Symbol	Conditions	🖉 min 🦯	typ	max	Unit
DAC resolution	RES		See See	16		bits
Total harmonic distortion	THD	For f = 1 kHz, 0 dB*1	and the second second		0.10	%
Dynamic range	DR	For f = 1 kHz, -60 dB	<i>§</i> 90	92		dB
Crosstalk	СТ	For f = 1 kHz, 0 dB	S. S		-85	dB
Signal-to-noise ratio	S/N	JIS-A	94	98		dB
Full-scale output voltage	VFS	- // <i>B</i> rr //	1.65	1.8	1.95	Vр-р
Power dissipation	Pd	*2		20	30	mW
Output load resistance	RL	Pins 21 and 23	30			kΩ

Note: 1. 0 dB means full scale.

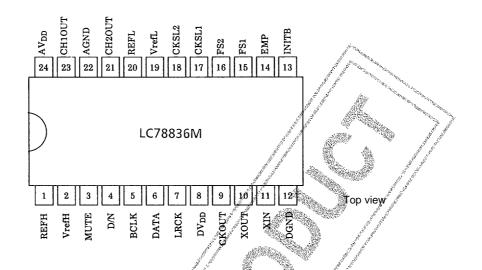
2. XIN amplitude (pin 11): 0.9 to 2.1 V,  $f_X = 16.9344$  MHz

The test circuit should be based on the sample application circuit.

#### **Block Diagram**



#### Pin Assignment



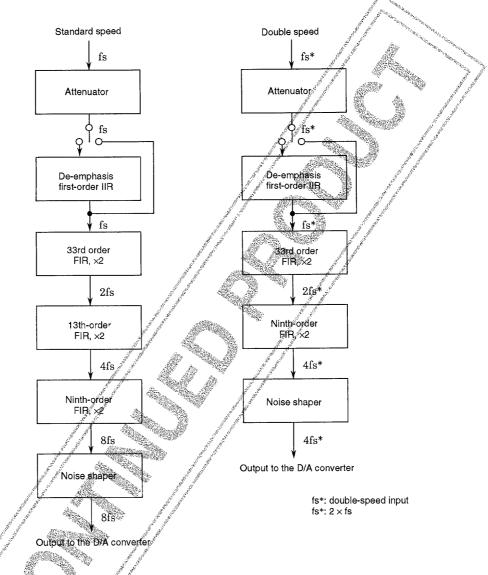
#### **Pin Functions**

Pin No.   Symbol   Federical     1   REFH   High-level reference voltage input     2   VrefH   High-level reference voltage input     3   MUTE   The soft mutuing function is turned on by a high-teput.     4   DN   Bioinder/double-speed operation wherhigh, standard depen tow     5   BCLK   Bit clock input     6   DATA   El clock input     7   LRCK   DH clock uppt     8   DVop   Digital audio data input     9   CKOUT   DH clock uppt     9   CKOUT   Inder/mbles pride complete at 198 fs. clock input     11   XIN   Crystal product system power supply     12   DOND   Digital system power supply     9   CKOUT   Inder/mdes/mdes/mdes/mdes/mdes/mdes/mdes/mdes								
1   KHH   Normally connected through a capacitor to ASND.     2   VrefH   High-level reference voltage input     3   MUTE   Muting signal input     4   D/N   Standard/double-speed mode synking inguit     5   BCLK   Bit clock input     6   DATA   Diptial audio data input     7   LRCk   LR clock input     8   DVpp   Diptial system forwer supply     9   CKOUT   in 392 ker profer supply     11   XIN   Crystal profilence to the speed node system forwer supply     12   Dobb profers supply   Diptial system forwer supply     13   INTB   Trialization speed mode system forwer supply     14   EM   Crystal profilence to the speed mode system forwer supply     13   INTB   Trialization speed mode system forwer supply is set to speed mode system forwer supply is set to speed mode system forwer supply     14   EM   Deremposes titter (system clock subply in profilence to the speed mode system forwer supply is set to speed mode system forwer supply     15   PS1   V   H   H     16   FS2   V   H   H   H	Pin No.	Symbol	Function					
3   Mutter The soft muting function is turned on by a high-input.     4   D/N   Standard/double-speed mode switching input Double-speed operation when high, standard when have     5   BCLK   Bit clock input     6   DATA   Digital subscience speed mode switching input Input is in a twos-complement MSR ites torinat.     7   LR clock input   Digital system cover supply     8   DV_DD   Digital system cover supply     9   CKOUT   In other/modes outputs a 196 ts clock in other/modes outputs a 196 ts clock output in 392 ts prodei outputs a 196 ts clock output in 392 ts prodei curputs a 196 ts clock output in 0 ther/modes outputs a 196 ts clock output in 392 ts prodei curputs a growther clock output in 392 ts prodei curput (system clock output)     10   XOUT   Crystal pscillator burgut (system clock output)     11   XIN   Crystal pscillator burgut (system clock /ipdi)     12   DGND   Digital system growther in the is turged on when his pri is set low.     13   INTB   Filte is turged on when his pri is set low.     15   FS1   L   H   L     16   FS2   L   H   H   L     17   CKSL1   CKSL2   System clock   System clock   System clock	1	REFH						
3   MUTE   The soft muting function is turned of by is high-troput.     4   DN   Standard/double-speed mode switching input     5   BCLK   Bit clock input     6   DATA   Digital audio data input   Digital audio data input     7   LRCK   LR clock input   Digital system optimation is turned of by is high cH2 when low.     8   DVop   Digital system power supply   Clock output   In also is high cH2 when low.     9   CKOUT   Clock output   Clock output   In also is high cH2 when low.     10   XOUT   Crystal oscillator couput (system clock aight)   Decimphase is a table is clock aight)     11   XIN   Crystal oscillator couput (system clock aight)   Decimphase is ther on/off sylfoping     12   DGND   Digital system ground   Yei H   H   L     13   NITF   Finitalization signal input (system clock aight)   Decimphase is ther on/off sylfoping     14   EMP   Decimphase if ther on/off sylfoping   H   H   L     16   FS2   L   L   H   H   L     17   CKSL1   CKSL1   System clock   System	2	VrefH	gh-level reference voltage input					
4   DN   Double-speed operation when high, standard when low     5   BCLK   Bit clock input     6   DATA   Digital audio data input / Input is in a twos-complement MSB-trist format     7   LRCK   LR clock input / Input is in a twos-complement MSB-trist format     8   DVpp   Digital audio data input / Input is in a twos-complement MSB-trist format     9   CKOUT   In out went this pin is high. CH2 when low.     10   XDU   Clock output / Input is a twos-complement MSB-trist format.     11   XIN   Clock output / Input is a twos-complement went is pin is high. CH2 when low.     10   XOUT   Crystal scillator shadu (system clock wind)     11   XIN   Crystal scillator input (system clock wind)     12   DGND   Digital audio this pin is set low.     13   INTB   Antialization spin (system clock wind)     14   EMP   De-emphasis filter on/cft switching     16   FS2   L   L   H   L     16   FS2   L   L   H   H   L     17   CKSL1   System clock   System clock   System clock   L   H   H	3	MUTE						
6 DATA Digital audio data input Input is in a twos-complement MSB-trist format   7 LRCK LR clock input CH is input when this pin is high. CH2 when low.   8 DV <sub>DD</sub> Digital system dower supply   9 CKOUT Clock output In 392 is frode: outputs a 196 is clock In other, modes: outputs a 206 k with the XIN frequency   10 XOUT Crystal oscillator input of clock output   11 XIN Cystal oscillator input of system clock output   12 DGND Digital system ground   13 INITB Initialization signal input file is surged on when this pin is set high, off when set low.   14 EMP De-emphasis filter on/off synthing The kiter is turged on when this pin is set high, off when set low.   15 FS1 V H   16 FS2 L L   17 CKSL1 CKSL1 System clock   18 OKSL2 L H H   19 VrefL Low-level reference voltage input   20 REFL Low-level reference voltage input   20 REFL Low-level reference voltage input   21 CH2OUT CH2 analog output   22 AGND Analog system ground	4	D/N						
6   DATA   Input is in a twos-complement MSEstist format     7   LRCK   LR clock input   LR clock input     8   DV <sub>DD</sub> Digital system power supply     9   CKOUT   In 32 (s proble: outputs) a 196 (s clock input)     10   XOUT   Crystal decillator butput (system clock with the XJN frequency In 332 (s proble: outputs) a 396 (s victork output)     11   XIN   Crystal decillator butput (system clock output)     12   DGND   Digital system grown     13   INITB   //initialization signal input     14   EMP   De-emphasis filter on/off synforing The Hiler is turned on when this pin is set ligh, off when set low.     15   FS1   PS2   L   H   H   L     16   FS2   L   L   H   H   L     17   CKSL1   System flook selection   System clock   L   H   H   L     18   CKSL2   H   L   48 kls   L   H   System clock     19   VrefL   Low-level reference voltage input   H   L   448 ls   H   L   H   H   L   L<	5	BCLK	Bit clock input					
7LRCkCH1 is input when this pin is high CH2 when low.8DV <sub>DD</sub> Digital system fower supply9CKOUTIn 32 is piofe: outputs a 196 is clock In other modes: outputs a took with the XIN trequency10XOUTCrystal oscillator builty (system clock output)11XINCystal oscillator builty (system clock output)12DGNDDigital system growth13INITBJritialization span al input14EMPDe-emphasis filter on/off sylfoping The lifer is turned on when this pin is set low.15FS1FS216FS2LL17CKSL1System clock FS218CKSL2System clock H19VrefLLow-level reference voltage Normally connected through a capacitor to AGND.20REFLLow-level reference voltage Normally connected through a capacitor to AGND.21CH2OUTCH2OUTCH2 analog output22AGNDAnalog system ground	6	DATA						
9CKOUTClock output In 392 fs prode: outputs a 196 fs clock In other, mixed expression196 fs clock In other, mixed expression10XOUTCrystal scillator, bulput (system clock sinput)11XINCrystal scillator, bulput (system clock sinput)12DGNDDigifal system ground13INITBInitialization signal mpot The LSI's sinualized when this pin is set low.14EMPDe-emphasis filter on/off switching The filter is turied on when this pin is set high, off when set low.15F51F5216F52LL17CKSL1System clock selection18CKSL1CKSL219VreftLow-level reference voltage input Low-level reference voltage Normally connected through a capacitor to AGND.20REFLLow-level reference voltage Normally connected through a capacitor to AGND.21CH2OUTCH2 analog output	7	LRCK						
9CKOUTIn 392 fs mode: outputs a 196 fs clock In other modes: outputs a clock with the XIN trequency10XOUTCrystal oscillator, butput (system clock output)11XINCrystal oscillator, butput (system clock output)12DGNDDigital system ground.13INITBInitialization signal import The LS its initialized when this pin is set low.14EMPDe-emphasis filter on/off switching The filter is turned on when this pin is set high, off when set low.15FS1FS2L16FS2LL17CKSL1FS2L18OrKsL2System clock also19VrefLLow-level reference voltage Normaly connected through a capacitor to AGND.20REFLLow-level reference voltage Normally connected through a capacitor to AGND.21CH2OUTCH2 analog output22AGNDAnalog system ground	8	DV <sub>DD</sub>	Digital system power supply					
11   XIN   Crydstal oscillator input (system clock input)     12   DGND   Digital system ground     13   INITB   Initialization signal input     13   INITB   Initialization signal input     14   EMP   De-emphasis filter on/off switching The filter is turged on when this pin is set high, off when set low.     15   FS1   De-emphasis filter mode (32, 44.1, or 48 kHz) selection     16   FS2   L   H   H     16   FS2   L   L   H   H     17   CKSL1   CKSL1   CKSL2   System clock   L   H   H     18   CKSL2   H   L   384 fs   L   H   H   System clock     19   VrefL   Low-level reference voltage input   100-level reference voltage input   Low-level reference voltage input     20   REFL   Low-level reference voltage input   Low-level reference voltage input     21   CH20UT   CH2 analog output   22   AGND   Analog system ground	9	СКОИТ	In 392 fs mode: outputs a 196 fs clock					
12 DGND Digital system ground   13 INITB Initialization signal input The LSH is initialized when this pin is set low.   14 EMP De-emphasis filter on/off switching The filter is turied on when this pin is set high, off when set low.   15 F51 De-emphasis filter on/off switching The filter is turied on when this pin is set high, off when set low.   16 FS2 L L H   16 FS2 L L H   16 FS2 L L H   17 CKSL1 CKSL2 System clock   18 CKSL2 H L 384 fs   19 VrefL Low-level reference voltage input   20 REFL Low-level reference voltage Normally connected through a capacitor to AGND.   21 CH20UT CH2 analog output	10	XOUT	Crystal oscillator output (system clock output)					
13 INITB Initialization signal import The LSH is initialized when this pin is set low.   14 EMP De-emphasis filter on/off switching The filter is turned on when this pin is set high, off when set low.   15 FS1 De-emphasis filter mode (32, 44.1, or 48 kHz) selection   16 FS2 L L   16 FS2 L L   17 CKSL1 FS2 L   18 CKSL2 VerfL CKSL1   19 VrefL Low-level reference voltage Normally connected through a capacitor to AGND.   21 CH2OUT CH2 analog output	11	XIN	Crystal oscillator input (system clock input)					
13 INTB The LST is initialized when this pin is set low.   14 EMP De-emphasis filter on/off switching The filter is turded on when this pin is set high, off when set low.   15 FS1   16 FS2   17 FS2   18 FS2   18 CKSL2   19 VrefL   19 VrefL   10 CH2oUT   20 REFL   20 REFL   20 REFL   20 REFL   20 CH2oUT   21 CH2oUT   22 AGND	12	DGND	Digital system ground					
14   EMF   The fitter is turned on when this pin is set high, off when set low.     15   FS1   Peremphasisfilter mode (32, 44.1, or 48 kHz) selection     16   FS2   L   L   H   H     17   CKSLt   System clock selection   System clock   Image: CKSLt   Image: CKSLt     18   CKSL2   H   L   448 fs   Image: CKSL2   H   L     19   VrefL   Low-level reference voltage input   Low-level reference voltage input   Image: CH2OUT   CH2OUT   CH2OUT   CH2OUT   CH2 analog output     20   REFL   CH2OUT   CH2 analog output   Image: CH2OUT   CH2 analog output     21   CH2OUT   CH2 analog output   Image: CH2OUT	13	INITB	Initialization signal input The LSt is initialized when this pin is set low.					
15FS1HHL16FS2LLHH16FS2LLHH16FS2LLHH16FS2LLHH16FS2LLHH17CKSLSystem clock selectionSystem clock18CKSL2LAlternative formation of the selection of the selection18CKSL2HL19VrefLLow-level reference voltage input20REFLLow-level reference voltage Normally connected through a capacitor to AGND.21CH2OUTCH2 analog output22AGNDAnalog system ground	14	EMP						
Image: FS2Image: LImage: LImage: HImage: H16FS2Image: LImage: LImage: HImage: H16FS2Image: LImage: LImage: HImage: H17CKSL1System clock selectionImage: CKSL1Image: CKSL217CKSL1CKSL2System clockImage: L18CKSL2Image: LImage: HImage: L19VrefLLow-level reference voltage input20REFLLow-level reference voltage Normally connected through a capacitor to AGND.21CH2OUTCH2 analog output22AGNDAnalog system ground	15	F\$1						
16 FS2 fs 44.1 kHz 32 kHz 48 kHz   System clock selection   17 CKSL1 CKSL2 System clock   18 CKSL2 H 1 392 fs   18 CKSL2 H 1 448 fs   19 VrefL Low-level reference voltage input   20 REFL Low-level reference voltage Normally connected through a capacitor to AGND.   21 CH2OUT CH2 analog output   22 AGND Analog system ground		and the second second						
IT   CKSL1   CKSL2   System clock     L   L   384 fs     L   H   392 fs     H   L   448 fs     H   H   512 fs     19   VrefL   Low-level reference voltage input     20   REFL   Low-level reference voltage Normally connected through a capacitor to AGND.     21   CH2OUT   CH2 analog output     22   AGND   Analog system ground	16	FS2						
IT   CKSL1   CKSL2   System clock     L   L   384 fs     L   H   392 fs     H   L   448 fs     H   H   512 fs     19   VrefL   Low-level reference voltage input     20   REFL   Low-level reference voltage Normally connected through a capacitor to AGND.     21   CH2OUT   CH2 analog output     22   AGND   Analog system ground	and a state of the		System dock selection					
Image: Construction of the system ground Image: Construction of the system ground   18 Cristical dialog system ground   18 Cristical dialog system ground	A TO	CKCI AN						
L H 392 fs   18 CKSL2 H L 448 fs   H L 448 fs   H H 512 fs   19 VrefL Low-level reference voltage input   20 REFL Low-level reference voltage knownally connected through a capacitor to AGND.   21 CH2OUT CH2 analog output   22 AGND Analog system ground	A DE	CKSLI						
H L 448 fs   H H 512 fs   19 VrefL Low-level reference voltage input   20 REFL Low-level reference voltage Normally connected through a capacitor to AGND.   21 CH2OUT CH2 analog output   22 AGND Analog system ground	Sector Sector							
H H 512 fs   19 VrefL Low-level reference voltage input   20 REFL Low-level reference voltage disput   21 CH2OUT CH2 analog output   22 AGND Analog system ground	June .							
Image: Section of the section of t	18	CKSL2						
20 REFL Low-level reference voltage Normally connected through a capacitor to AGND.   21 CH2OUT CH2 analog output   22 AGND Analog system ground	10	Vrofl						
20 REFL Normally connected through a capacitor to AGND.   21 CH2OUT CH2 analog output   22 AGND Analog system ground	13							
22 AGND Analog system ground	20	REFL						
	21		CH2 analog output					
23 CH1OUT CH1 analog output	22	AGND						
			CH1 analog output					
24 AV <sub>DD</sub> Analog system power supply	24	AV <sub>DD</sub>	Analog system power supply					

#### **Operating Description**

1. Digital Filters

The LC78836M performs the following calculations.



• Oversampling

The oversampling circuit consists of 2× interpolation filters (implemented as FIR filters) connected in series. In standard-speed operation, the circuit implements 8× oversampling by connecting three stages of FIR filters (33rd,13th, and ninth orders) in series. In double speed operation, the circuit implements 4× oversampling by connecting two stages of FIR filters (33rd and ninth orders) in series. See page 9 for the filter characteristics.

De-emphasis

The LC78836M implements digital de-emphasis with a first-order IIR filter. The filter coefficients correspond to sampling frequencies (fs) of 32, 44.1, and 48 kHz. (The frequencies are doubled in double-speed operation.) See page 10 for the filter characteristics when de-emphasis is on.

 De-emphasis on/off switching De-emphasis on/ EMP = high

De-emphasis off: EMP = low

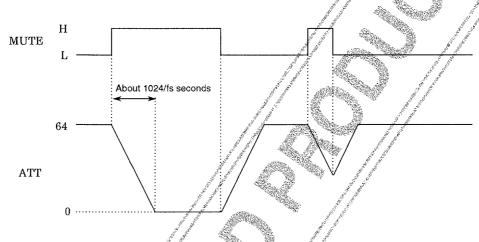
– Filter coefficient selection

FS1	L	Н	Н	L
FS2	L	L	Н	Н
fs	44.1	kHz	32 kHz	48 kHz

#### • Soft muting

Soft muting is implemented using the on-chip digital attenuator. The attenuator attenuation is given by the following formula. 20 Log (ATT/64) dB

Here, ATT is an integer between 0 and 64 inclusive. However, the attenuation is  $-\infty$  when ATT = 0. When the MUTE pin is set high, the ATT value is reduced one level at a time towards zero, and the attenuation changes, moving towards  $-\infty$ . When the MUTE pin is set low, the ATT value is increased one level at a time towards 64, and the attenuation changes, moving towards 0 dB. The time required for the soft mute function to complete is about 1024/fs.



• Noise shaper

The LC78836M uses a first-order noise shaper to reduce re-quantization noise in the output of the DF calculations. Double-speed support

Double-speed support

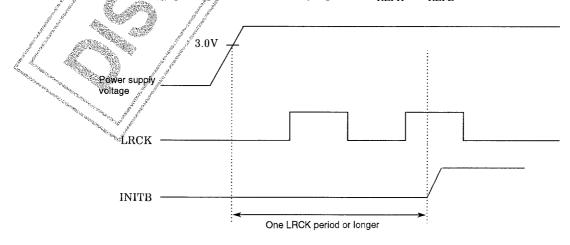
The LC78836M supports double-speed CD playback when the D/N pin is set high. In this mode, the BCLK, LRCK, and DATA inputs should be input with twice the frequencies they have in standard-speed mode. Note that the system clock (the XIN pin clock) has the same frequency as it does in standard-speed mode. The LC78836M supports double-speed operation when the system clock is a 384 fs or 512 fs clock, but does not support this mode for 392 fs and 448 fs clocks, Since the LC78836M enters test mode for these settings, they should not be used.

Standard-speed mode; D/N pin = low

Double-speed mode: D/N pin = high

2. Initialization

The LC78836M must be initialized when power is first applied or when the system clock is switched. Initialization is executed by setting the INITB pin low. While that pin is low, after the power supply voltage stabilizes, input the XIN, BCLK, and LRCK signals, and wait at least one LRCK period, as shown in the figure below. When INITB is low, all 16 bits of the digital filter outputs will be zeros, and the D/A converter outputs (CH10UT and CH20UT) will be analog 0 (a potential essentially equal to  $(V_{REFH} + V_{REFL})/2$ ).



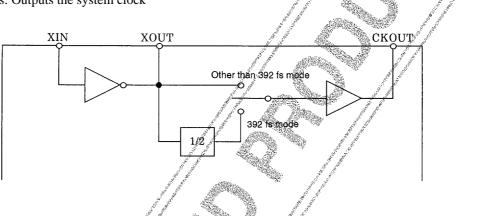
#### 3. System Clock

The LC78836M supports four system clocks: 384 fs, 392 fs, 448 fs, and 512 fs. The CKSL1 and CKSL2 pins select the clock used.

CKSL1	CKSL2	System clock
L	L	384 fs
L	н	392 fs
Н	L	448 fs
н	н	512 fs

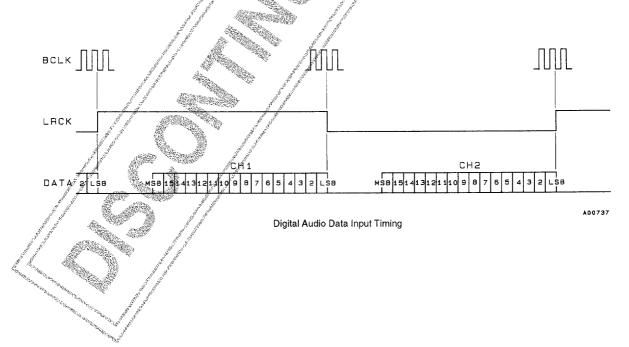
• CKOUT pin

For a 392 fs clock: Outputs a 196 fs clock (system clock/2) All other clocks: Outputs the system clock



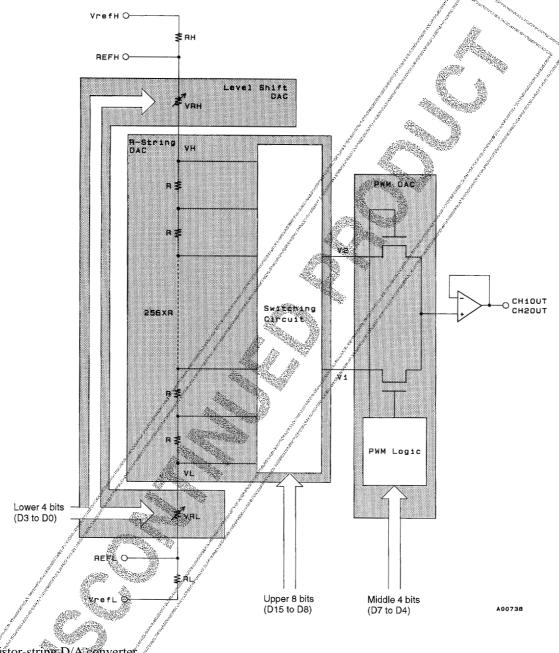
4. Digital Audio Data Input

The digital audio data is a 16-bit serial signal in an msb-first twos complement format. The 16-bit serial data is input from the DATA pin to an internal register on the rising edge of BCLK, and is latched on the next LRCK rising or falling edge.



#### 5. D/A Converter Block

The LC78836M incorporates an independent 16-bit D/A converter and an operational amplifier for signal output for each channel (CH1 and CH2). It adopts a dynamic level shifting conversion technique that uses a resistor-string D/A converter, a PWM (pulse width modulation) D/A converter, and a level shifting D/A converter, (See figure.)



• Resistor-string D/A converter

This is an 8-bit D/A converter in which a total of  $256 (= 2^8)$  unit-resistance resistors are connected in series and the potential applied to the ends of that resistor string is voltage divided into 256 equal intervals. Of these resistordivided potentials, two adjacent potentials, V1 and V2, are selected by a switching circuit according to the value of the upper 8 bits of the data. These two potentials are output to the PWM D/A converter. Note that these potentials are related as follows:

V2 - V1 = (VH - VL)/256

• PWM D/A converter

This is a 4-bit D/A converter that divides (by 16) the interval between the two potentials, V1 and V2, output by the resistor-string D/A converter. This circuit outputs one or the other of the V1 and V2 potentials from the CH1OUT (or CH2OUT) pin according to the value of the middle 4 bits of the data (D7 to D4).

• Level shifting D/A converter

This 4-bit D/A converter is implemented by connecting the variable resistors VRH and VRL in series at the ends of the resistor-string D/A converter resistors. The values of the VRH and VRL variable resistors are modified according to the value of the low-order 4 bits of the data (D3 to D0) as follows:

- The value of VRH + VRL is held fixed regardless of the value of the data.
- The values of VRH and VRL are changed in R/256 unit steps (where R is the value of the resistor-string D/A converter unit resistors) over the range zero to 15·R/256.

This causes the resistor-string D/A converter V1 and V2 outputs to change in  $\Delta V/256$  steps (where  $\Delta V = (VH - VL)/256$ ) over the range 0 to  $63 \times \Delta V/256$  according to the value of the lower 4 bits of the data.

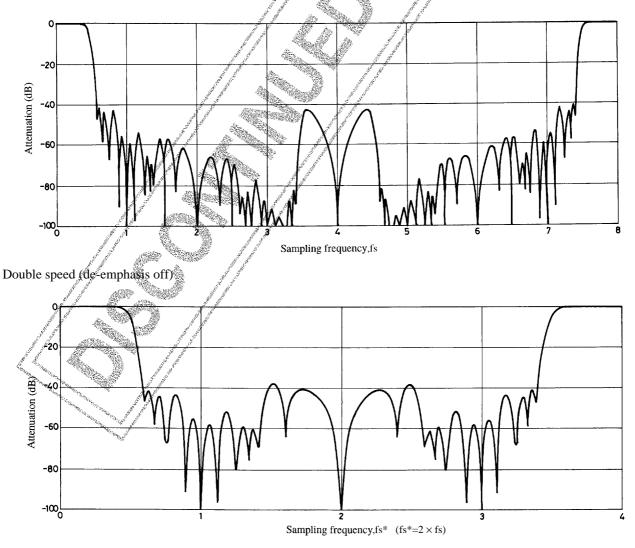
• VrefH/L and REFH/L pins The VrefH/L pins, which provide a reference voltage to the resistor string, are normally set to VrefH =  $AV_{DD}$  and VrefL = AGND. Note that capacitors (about 10 µF) should be connected between REFH and AGND and between REFL and AGND.

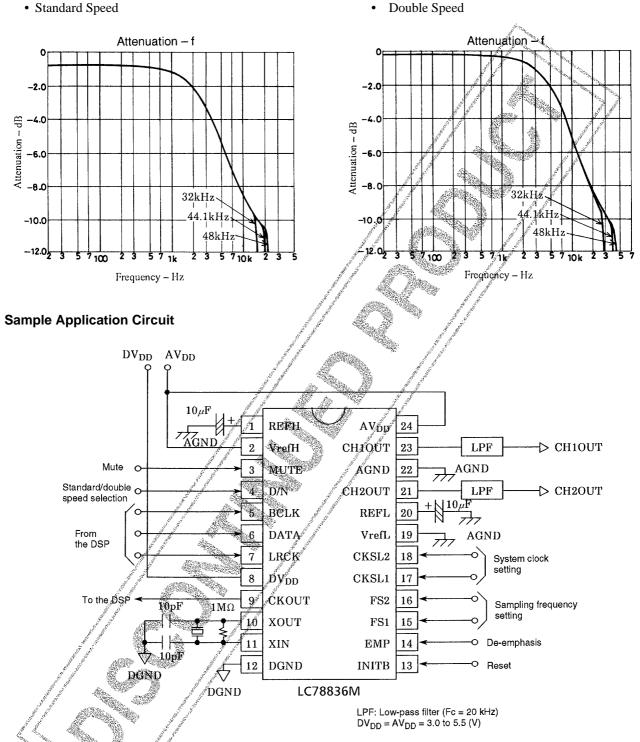
When VrefH is 5.0 V and VrefL is 0 V, the LC78836M outputs its maximum output amplitude as the range 0.5 V (minimum) to 3.5 V (maximum) (3.0 Vp-p) for 0 dB playback according to the built-in RH and RL resistors.

#### Filter Characteristics (logical values)

Standard speed:  $8 \times$  oversampling Double speed:  $4 \times$  oversampling Ripple: Less than  $\pm 0.1$  dB Attenuation: -40 dB or lower

Standard speed (de-emphasis off)





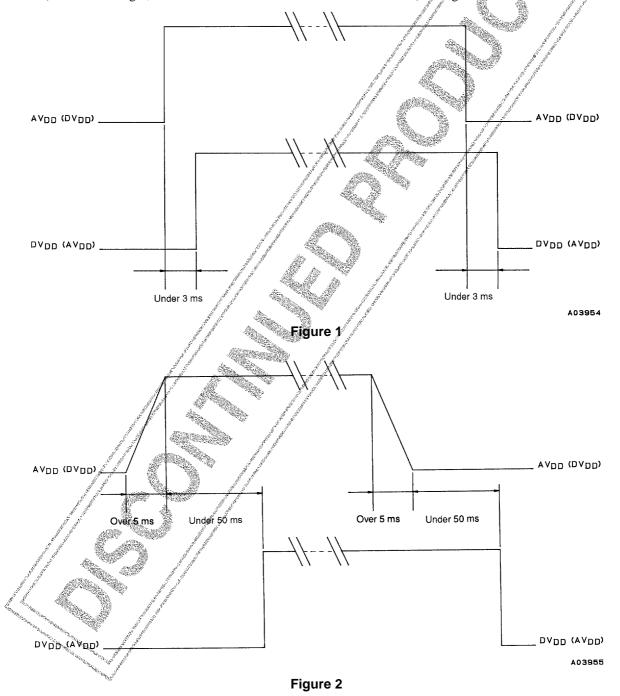
#### **De-Emphasis ON Transient Bandwidth Characteristics**

Note: 1. In the diagram, DV<sub>DD</sub> and DGND are for the digital system, and AV<sub>DD</sub> and AGND are for the analog system. DGND and AGND must be connected to the digital system and analog system grounds, respectively.

- 2. A low-impedance high-stability power supply (equivalent to a commercial three-terminal regulator) must be used for AV<sub>DD</sub> and VrefH.
- Since latchup can occur if there is a discrepancy in the pin 8 (DV<sub>DD</sub>) and pin 24 (AV<sub>DD</sub>) power supply voltage application timing, application circuits should be designed so that the pin 8 and pin 24 power supply voltages are applied at the same time.
- 4. Provide the XIN pm clock input quickly after power is applied. The IC may be destroyed if the XIN pin is held fixed at either the high or low level when power is applied.

#### **Power Supply Application Timing**

- 1. The analog power supply  $(AV_{DD})$  and the digital power supply  $(DV_{DD})$  must be turned on at the same time and must be turned off at the same time.
- 2. If discrepancies in the analog and digital power supply timings cannot be avoided, the timings must fulfill the following conditions.
  - The difference between times when the power supplies rise must be 3 ms or shorter. (See Figure 1)
  - If the time difference is greater than 3 ms, then the power supply that rises (falls) first must have a rise time (fall time) of 5 ms or longer, and the time difference must be less than 50 ms. (See Figure 2)



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